CLAIMS

What is claimed is:

1. A magnetic random access memory array comprising:

a plurality of magnetic storage cells;

a plurality of global word lines;

a plurality of word line segments, each of the plurality of word line segments being coupled with at least one of the plurality of global word lines such that the plurality of word line segments is selectable, each of the plurality of word line segments being coupled to a first portion of the plurality of magnetic storage cells {Stone, I replaced the "first portion" because otherwise the claim would read that each segment is coupled to all of the magnetic storage cells, which is not correct. Instead, each segment is coupled to some of the magnetic storage cells};

a plurality of global bit lines;

a plurality of bit line segments, each of the plurality of bit line segments being coupled with at least one of the plurality of global bit lines such the plurality of bit line segments is selectable, each of the plurality of bit line segments residing in proximity to a second portion of the plurality of magnetic storage cells to write to the second portion ofthe plurality of magnetic storage cells{Stone, I put back the "second portion" for the same reason as above. Each bit line segment is only coupled to some of the magnetic storage cells in the memory, not all of them}; and

a plurality of selection devices, the plurality of bit line segments and the plurality of

word line segments being coupled with and selectable using the plurality of selection devices.

2. The magnetic random access memory array of claim 1 wherein the plurality of global bit lines is substantially parallel to the plurality of global word lines.

3. The magnetic random access memory of claim 1 further comprising:

at least one global word line return coupled with at least one of the plurality of global word lines through at least one selection device.

4. The magnetic random access memory array of claim 3 wherein the at least one global word line return further includes a plurality of global word line returns.

5. The magnetic random access memory array of claim 4 wherein each of the plurality of global word line returns corresponds to one of the plurality of global word lines.

6. The magnetic random access memory of claim 1 further comprising:

at least one global bit line return coupled with at least one of the plurality of global bit lines through at least one of the plurality of selection devices.

7. The magnetic random access memory array of claim 6 wherein the at least

one global bit line return further includes a plurality of global bit line returns.

8. The magnetic random access memory array of claim 7 wherein each of the plurality of global bit line returns corresponds to one of the plurality of global bit lines.

9. The magnetic random access memory of claim 1 wherein at least a portion of the plurality of word line segments is magnetic.

10. The magnetic random access memory of claim 1 wherein at least a portion of the plurality of bit line segments is magnetic.

11. The magnetic random access memory array of claim 1 wherein the plurality of global bit lines have a lower resistance than the plurality of bit line segments.

12. The magnetic random access memory array of claim 1 wherein the plurality of global word lines have a lower resistance than the plurality of word line segments.

13 The magnetic random access memory array of claim 12 wherein each of the plurality of global word line segments has a thickness and a width, the thickness being less than the width.

14. The magnetic random access memory array of claim 13 wherein the thickness is less than or equal to one fourth of the width.

15. The magnetic random access memory array of claim 1 wherein the plurality of global bit lines and the plurality of global word lines are both manufactured on a particular metal layer.

16. The magnetic random access memory array of claim 1 wherein the plurality of selection devices include a plurality of transistors or a plurality of diodes

17. The magnetic random access memory array of claim 1 wherein each of the plurality of magnetic storage cells includes a magnetic tunneling junction including a free layer, a barrier layer, and a pinned layer, the plurality of word line segments being magnetically coupled with the free layer in each of the first portion of the magnetic storage cells.

18. A method for utilizing a magnetic random access memory array having a plurality of magnetic storage cells and a plurality of global word lines, the method comprising:

(a) in a write mode, driving a word line current through at least one of the

plurality of global word lines,

(b) in the write mode, driving at least a portion of the word line current from the at least one of the plurality of global word liens through at least one of a plurality of word line segments, each of the plurality of word line segments being coupled with a portion of the plurality of global word lines such that the plurality of word line segments is separately selectable, each of the plurality of word line segments being coupled to a first portion of the plurality of magnetic storage cells;

(c) in the write mode, driving a bit line current through at least one of a plurality of global bit lines; and

(d) in the write mode, providing at least a portion of the bit line current through a portion of a plurality of bit line segments, each of the plurality of bit line segments being coupled with at least one of the plurality of global bit lines such that the plurality of bit line segments is selectable, each of the plurality of segments residing in proximity to a second portion of the plurality of magnetic storage cells to write to the second portion of the plurality of magnetic storage cells;

wherein the plurality of bit line segments and the plurality of word line segments are coupled with and selectable using the plurality of selection devices.

19. The method of claim 18 further comprising the steps of:

(e) in a read mode, grounding a global word line, the read mode for reading a portion of the plurality of magnetic storage device;

(f) in the read mode, providing a read current in a portion of the plurality of global bit lines;

(g) in the read mode, providing the read current in a portion of the plurality of bit line segments; and

(h) in the read mode, reading a voltage across a portion of the plurality magnetic storage cells.

20. The method of claim 18 wherein the global word line driving step (a) further comprises:

(a1) utilizing at least one global word line return coupled with at least one of the plurality of global word lines through at least one selection device to return the word line current.

21. The method of claim 18 wherein the global bit line driving step (c) further comprises:

(c1) utilizing at least one global bit line return coupled with at least one of the plurality of global bit lines through at least one selection device to return the bit line current.

22. The method of claim 18 wherein at least a portion of the plurality of word line segments is magnetic.

23. The method of claim 18 wherein at least a portion of the plurality of bit line segments is magnetic.

24. The method of claim 18 wherein the plurality of global bit lines have a lower resistance than the plurality of bit line segments.

25. The method of claim 18 wherein the plurality of global word lines have a lower resistance than the plurality of word line segments.

26. The method of claim 18 wherein the plurality of global bit lines and the plurality of global word lines are both manufactured on a particular metal layer.

27. The method of claim 18 wherein each of the plurality of magnetic storage cells includes a magnetic tunneling junction including a free layer, a barrier layer, and a pinned layer, the plurality of word line segments being magnetically coupled with the free layer in each of the first portion of the magnetic storage cells.

28. A method of providing a magnetic random access memory array comprising:

(a) providing a plurality of magnetic storage cells;

(b) providing a plurality of global word lines;

(c) providing a plurality of word line segments, each of the plurality of word line segments being coupled with at least one of the plurality of global word lines such that the plurality of word line segments is selectable, each of the plurality of word line segments being coupled to a first portion of the plurality of magnetic storage cells;

(d) providing a plurality of global bit lines;

(e) providing a plurality of bit line segments, each of the plurality of bit line segments being coupled with at least one of the plurality of global bit lines such the plurality of bit line segments is selectable, each of the plurality of bit line segments residing in proximity to a second portion of the plurality of magnetic storage cells to write to the second portion of the plurality of magnetic storage cells; and

(f) providing a plurality of selection devices, the plurality of bit line segments and the plurality of word line segments being coupled with and selectable using the plurality of selection devices.